Improved Heat Dissipation and Optical Performance of High-power LED Packaging with Sintered Nanosilver Die-attach Material

Paul Panaccione[1], Tao Wang[2,3], Xu Chen[3], Susan Luo[4], and Guo-Quan Lu[2]
[1] Luminus Devices Inc., 1100 Technology Park Dr., Billerica, MA 01821
[2] Dept. of MSE, Virginia Tech, 213 Holden Hall, Blacksburg, VA 24061
[3] School of Chemical Engineering, Tianjin Univ., Tianjin, China
[4] NBE Technologies, LLC, 2200 Kraft Dr., Suite 1425, Blacksburg, VA 24060
ppanaccione@luminus.com

Abstract

Heat removal in packaged high-power light-emitting diode (LED) chips is critical to device performance and reliability. Thermal performance of LEDs is important in that lowered junction temperatures extend the LED's lifetime at a given photometric flux (brightness). Optionally, lower thermal resistance can enable increased brightness operation without exceeding the maximum allowable Tj for a given lifetime. A significant portion of the junction-to-case thermal resistance comes from the joint between chip and substrate, or the die-attach layer. In this study, we evaluated three different types of leading die-attach materials; silver epoxy, lead-free solder, and an emerging nanosilver paste. Each of the three was processed via their respective physical and chemical mechanisms: epoxy curing by cross-linking of polymer molecules; intermetalic soldering by reflow and solidification; and nanosilver sintering by solid-state atomic diffusion. High-power LED chips with a range of chip areas from 3.9 mm^2 to 9.0 mm^2 were attached by the three types of materials onto metalized aluminum nitride substrates, wire-bonded, and then tested in an electro-optical setup. The junction-to-heatsink thermal resistance of each LED assembly was determined by the wavelength shift methodology. We found that the average thermal resistance in the chips attached by the nanosilver paste was the lowest, and it was highest from the chips attached by the silver epoxy. For the 3.9 mm^2 die, the difference was about 0.6^{o}C/W, while the difference between the sintered and soldered was about 0.3^{o}C/W. The lower thermal resistance in the sintered joints is expected to significantly improve the photometric flux from the device. Simple calculations, excluding high current efficiency droop, predict that the brightness improvement could be as high as 50% for the 3.9 mm^2 chip. The samples will be functionally tested at high current, in both steady-state and pulsed operation, to determine brightness improvements, including the impact of droop. Nanosilver die-attach on a range of chip sizes up to 12 mm^2 are also considered and discussed.

Key words: nano-silver, die-attach, LED

I. INTRODUCTION

High brightness LEDs are being designed into many high flux applications which previously have been dominated by various types of light bulbs. High brightness LED applications include high efficiency general lighting and high performance projection display where brightness is critical. In display applications, LEDs are used to replace mercury arc lamps, and are often driven at their maximum allowable power levels and operating temperatures, so projector LEDs will be discussed in this paper to demonstrate the thermal benefits and brightness benefits of a low-temperature sinterable nanosilver die-attach material compared to other conventional die-attach materials such as Ag-epoxy or solder. A typical configuration for projector light engines is to use a set of red, green and blue LEDs, with red and green being of primary concern with respect to brightness, while blue has typically neither a brightness nor a thermal bottleneck.

A. Luminus Devices LED Background

A variety of illumination and projection applications previously thought impossible for solid state lighting are now being realized with Luminus Devices' "big chip" PhlatLight® devices. Luminus' big chip LEDs are used for both projection display and illumination applications that require high brightness. PhlatLight LEDs are currently being used in projection light engines, and a variety of other lighting applications that require high brightness and efficiency, wide color gamut, high color rendering, and long lifetimes. Luminus line of projection LEDs has been developed and enhanced for projection applications by providing large, uniform emitting areas with collimated light extraction, and geometries well matched to projection aspect ratios. The LED package design has also been developed to address projection applications, particularly with respect to thermal dissipation. In the current platform, the chip is attached with a high conductivity Ag-epoxy directly to a copper heatspreader package. The

current Ag-epoxy has an industry leading bulk conductivity of 60W/mK. Taking the interface resistances into account, we realize an effective conductivity of 20W/mK.

$$Rth=Rth(bulk)+Rth(interface1)+Rth(interface2) \quad (1)$$

A common alternative to Ag-epoxy die attachment is solder. Some of the challenges of solders are that they can require a higher temperature and slower process, and can be subject to formation of brittle intermetallics and fatigue fracture. With proper design and processing, solders can produce a reliable joint, but their bulk thermal conductivities are not significantly different than a highly loaded 90% Ag-epoxy. Table 1 shows process temperatures and bulk conductivities of some common solders and Ag-epoxies.

Material	Process Temperature (deg.C)	Bulk Thermal Conductivity (W/mK)
90% Ag-epoxy	225	60
86% Ag-epoxy	200	12
80Au/20Sn	>280	57
96.5Sn/3.5Ag	>221	33
SN100C Sn/0.7Cu/0.05Ni+Ge	>227	64
Sintered nano-Ag	~260	240

Table 1: TIM1 comparison

B. NBE Tech Nanosilver Background

Also shown in Table 1 are the process temperature and bulk thermal conductivity of a nanosilver die-attach paste. The material has been developed by NBE Tech for the low-temperature joining technique (LTJT), an emerging die-attach method pioneered by researchers in the power electronics industry [1-6]. For power electronics module packaging, the LTJT die-attach has been shown to offer 3x better electrical performance, 5x temperature-cycling reliability, and higher device junction temperature up to 175°C [7,8]. The traditional LTJT die-attach process uses a micro-sized silver paste and requires pressure between 30 MPa and 40 MPa to lower the sintering temperature. NBE's nanosilver paste or nanoTach®, can be sintered at low temperature without pressure [9-12], which significantly simplifies implementation of the LTJT in manufacturing. The sintered silver joint offers an order of magnitude improvement in thermal performance over Ag-epoxies and solders, providing a bulk conductivity of 240W/mK. And by employing Ag surfaces on the die backside and on the package substrate, interface resistances are eliminated by direct Ag to Ag atomic diffusion during sintering.

II. MOTIVATION FOR USING NANOSILVER DIE-ATTACH IN LED PACKAGING

The primary motivation for using nano-Ag die attach material in high brightness LEDs for projection applications is to lower the package thermal resistance, which allows us to then drive the LED at a higher current without increasing Tj, thus producing higher light output. Another benefit of lowered thermal resistance from nano-Ag die attach is that it enables a lower Tj at the same brightness, resulting in enhanced reliability.

A. Thermal calculations

Calculations of potential thermal improvements for several chip sizes were conducted over a range of TIM1 thermal conductivities. The calculated results are shown in figure 1. The calculations predict that there is significant opportunity for further reduction of package thermal resistance by increasing the TIM1 thermal conductivity beyond the current effective conductivity of 20W/mK to greater than 100W/mK, at which point the opportunity approaches optimization. This thermal improvement cannot be achieved by solder, however nano-Ag's conductivity would bring us well into the flat region of the curve, thus optimizing the TIM1 to its maximum potential.

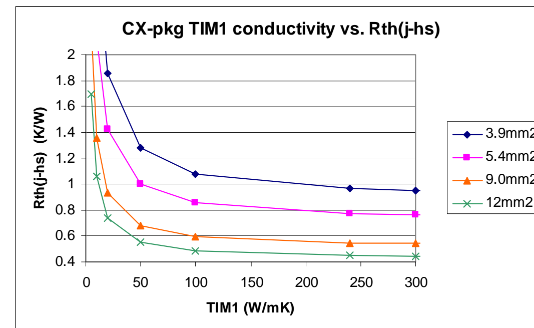

Fig. 1: Package Rth for a range of chip sizes and TIM1 conductivities

Focusing on just the difference between the current 20W/mK Ag-epoxy and the 240W/mK nano-Ag, we calculate a potential reduction in thermal resistance of approximately 0.3 C/W to 0.9 C/W for a range of die sizes from 12mm^2 to 3.9mm^2 respectively. This is illustrated figure 2 and table 2.

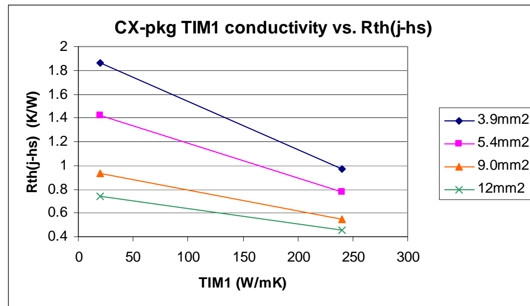

Fig. 2: Package Rth potential improvement

	PT39CX	PT54CX	CBT90	PT120CX	
TIM1	Rth(j-hs)	Rth(j-hs)	Rth(j-hs)	Rth(j-hs)	
W/mK	K/W	K/W	K/W	K/W	
20	1.86	1.42	0.94	0.74	90%Ag-epoxy
240	0.97	0.78	0.55	0.45	nano-Ag
	0.89	0.65	0.39	0.29	K/W improvement

Table 2: Package Rth potential improvement

III. EXPERIMENTATION

In this study, we examined the thermal performances of PhlatLight® Big Chip LEDs. The chips were metalized with 1000 Å-Ti/5000 Å-Ag on the backside. LED chips were attached onto Ag-plated metalized aluminum nitride DPC (Direct Plated Copper) substrates using three different types of lead-free die-attach materials for comparison: (1) silver-filled epoxies, one with 86% Ag loading and one with 90% Ag loading; (2) SN100C (Sn-0.7Cu-0.05Ni+Ge) and SAC305 solder preforms; and (3) nanosilver paste from NBE Technologies, LLC under the trade name of nanoTach®. Each die-attachment was processed via their respective physical and chemical mechanisms: epoxy curing by cross-linking of polymer molecules; intermetalic soldering by reflow and solidification; and nanosilver sintering by solid-state atomic diffusion, respectively.

In order to prepare silver epoxy glued LED devices, silver epoxy was dispensed onto the Ag-plated package substrate first, and then the LED chip was placed onto the dispensed epoxy using pick and place tool for further curing process.

Vacuum solder reflow was employed for soldered LED samples in a vacuum reflow chamber. The environment pressure was set to less than 7.0 x 10^{-6} MPa during reflow. A weight of 1 gram was applied onto LED chips to make a good initial contact between the solder preform and LED/substrate. Forming gas (95% N2/5% H2) was employed to remove oxidation on the solder preform.

For the silver sintered LED devices, the low-temperature joining technology (LTJT) by nanosilver sintering was used to mount the semiconductor device on the metalized substrate [17]. Low temperature sintering is enabled as the particle surface area to volume ratio becomes large enough to cause the surface energy to increase such that atomic diffusion is enabled at a lower temperature than on larger scale particles.

The junction-to-heatsink thermal resistance of each LED assembly was determined by the wavelength shift methodology, in which peak wavelength shift of LEDs has been correlated to a change in junction temperature [13,14].

Cross-sections of the various die attach bondlines are illustrated in the SEM images in fig. 3.

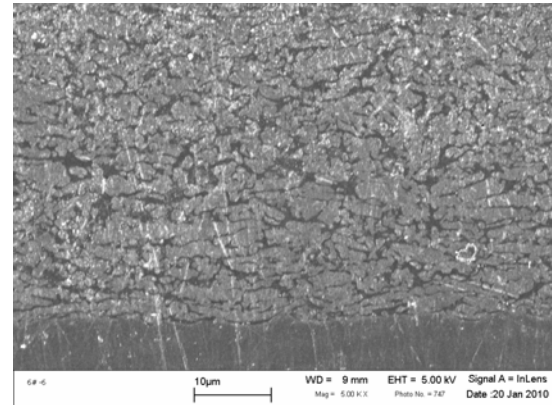

Fig. 3a: 90%Ag-epoxy

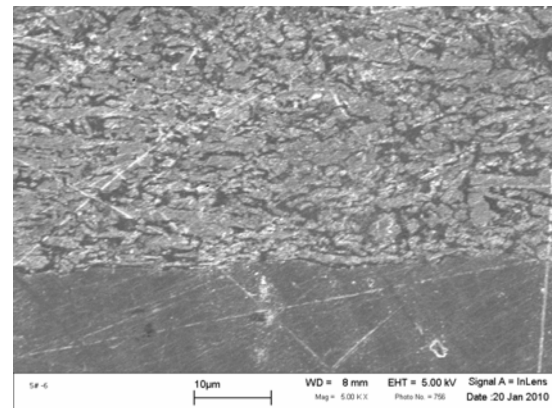

Fig. 3b: 86%Ag-epoxy

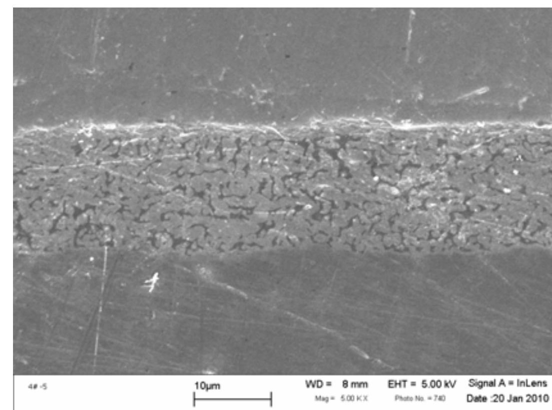

Fig. 3c: sintered nano-Ag

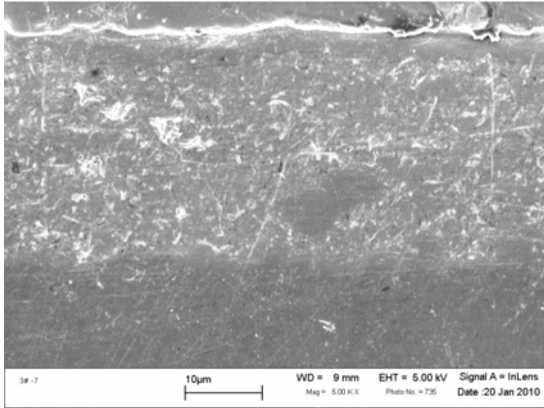

Fig. 3d: SN100C solder

IV. EXPERIMENTAL RESULTS

Evaluation devices were built with three different die sizes, and several different die-attach materials, including Ag-epoxies, solders, and sinterable nanosilver paste. Thermal resistance and shear strength were measured.

The test package structure was a 0.5mm thick aluminum nitride ceramic substrate with 2 ounce (70um) Cu circuit traces on both sides. This ceramic substrate was selected for the test structure because it has Ag plated circuit traces, which are ideal for sintering of the nano-Ag paste. The die backside was also prepared with Ag evaporated onto the backside. After the die was attached to the ceramic substrate, it was wirebonded then surface mounted onto an aluminum core PCB and bolted to a 40deg.C heatsink for thermal measurements. The assembled LED device is shown in Fig. 4.

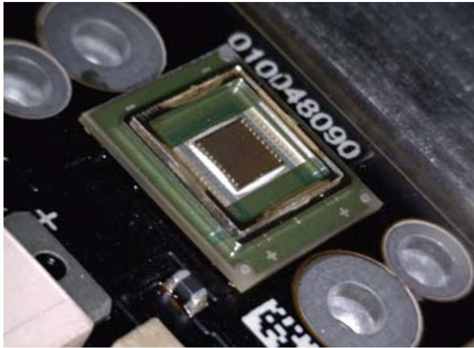

Fig. 4a: LED for thermal test

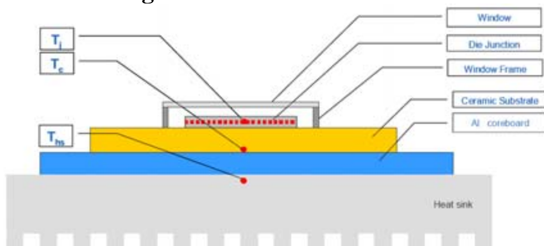

Fig. 4b: cross-section of test structure

A. Thermal performance results

Thermal testing was performed using the wavelength shift method. This methodology allows us to use light to measure the device junction temperature by correlating wavelength shift (delta lambda) to temperature shift (delta Tj). AlInGaP devices are particularly well suited for this method due to their linear response for delta lambda versus delta T. The measured results are shown in table 3.

	3.9mm^2 die	9.0mm^2 die
86%Ag-epoxy	2.72 C/W	1.7 C/W
SN100C	2.39 C/W	
SAC305	2.24 C/W	
sintered nano-Ag	2.14 C/W	1.5 C/W

Table 3: Rth measurements

Thermal measurements resulted in a 0.6deg.C/W reduction in thermal resistance for the 3.9mm^2 die, and a 0.2deg.C/W improvement for the 9.0mm^2 die; about 2/3 of the calculated improvement.

B. Brightness

Using the thermal measurement results, we can next calculate the potential brightness improvement for the range of chip sizes. The die junction temperature, Tj, is the limiting factor for projection applications, so we will hold Tj constant, and allow the operating current, I(in), to increase as it is inversely proportional to the thermal resistance (Rth).

$$Rth=[Tj(initial)-Tj(final)]/[VfxI(in)-P(optical)] \quad (2)$$

Initial brightness calculations will assume steady-state operation and no droop. We will conduct experiments later to empirically determine the effect of droop in both steady-state and pulsed operation. Droop refers to an LED phenomenon where photometric flux increases asymptotically as a function of current density to a peak brightness, then reverses direction and brightness actually decreases at higher current densities. So at high current densities, it is expected that droop may counteract the brightness opportunity to some degree.

Calculations using formula (2) below predict that the potential brightness improvement, excluding droop, could be as high as 30% to 50% for the 3.9mm^2 to 9mm^2 chip range.

$$\phi' = P'(\phi/P) \quad (2)$$

where:
ϕ' = photometric flux with nano-Ag
ϕ = photometric flux with Ag-epoxy
P' = input electrical power with nano-Ag
P = input power with Ag-epoxy

Table 4 shows the brightness calculation results for a range of chip sizes, at a fixed junction temperature in steady-state operation, and excluding droop. Red and green chips are studied, because in red/green/blue LED projection applications blue is typically not a brightness bottleneck.

RED			
emitting area	datasheet	nano-Ag	improvement
mm^2	lumens	lumens	%
3.9	310	465	50%
9.0	650	836	29%

GREEN			
emitting area	datasheet	nano-Ag	improvement
mm^2	lumens	lumens	%
3.9	770	1155	50%
9.0	1650	2121	29%

Table 4: Potential brightness excluding droop

C. Mechanical performance

Mechanical strength of the various TIM1s was tested by shearing the die from its package substrate, measuring the shear force, then calculating the shear strength ($\sigma = F/A$). Two die sizes were tested. Sintered nano-Ag exhibited the highest shear strength of the various TIM1s tested. The results are shown in table 5.

	3.9mm^2 die	5.4mm^2 die
86% Ag-epoxy	38 MPa	29 MPa
SN100C	53 MPa	33 MPa
sintered nano-Ag	64 MPa	44 MPa

Table 5: shear strength measurements

Thermal cycling was performed on 6 pieces from -40C to +125C for 55 cycles. Thermal resistance was measured before and after, and no change was detected. Nano-silver paste has a modulus of elasticity of 10 GPa versus 60 GPa for SN100C solder, so it is expected to be more resistant to cyclic fatigue fracture.

V. SUMMARY

A significant improvement in Rth has been demonstrated; 0.6C/W reduction in thermal resistance for 3.9mm^2 die, and a 0.2C/W improvement for 9.0mm^2 die.

Superior shear strength and resistance to thermal cycling fatigue have also been demonstrated empirically.

Next, a variety of die sizes and colors will be assembled and photometric flux will be tested over a range of current densities (J) to empirically evaluate the actual brightness improvement, including the impact of droop.

ACKNOWLEDGEMENTS

The authors would like to thank Rommanie Kuch of Luminus Devices for performing thermal resistance testing and optical testing.

REFERENCES

1. Crane, C.H., D. T. Lovell, W. A. Baginski, and M. G. Olsen, *Diffusion welding of dissimilar metals.* Welding Res. Supp., 1967. **46**: p. 23-31.
2. O'Brian, M., C. R. Rice, and D. L. Olsen, *High strength diffusion welding of silver coated base metals.* Weld. J., 1976. **55**(1): p. 25-27.
3. Scheuermann, U., *Low Temperature Joining Technology - A High Reliability Alternative to Solder Contacts*, in *Workshop on Metal Ceramic Composites for Functional Application*. 1997: Vienna.
4. Schwarzbauer, H., and Kuhnert, R. , *Novel large area joining technique for improved power device performance.* IEEE Trans. Ind. Appl., 1991. **27**: p. 93-95.
5. Amro, R., J. Lutz, J. Rudzki, R. Sittig, and M. Thoben. *Power Cycling at High Temperature Swings of Modules with Low Temperature Joining Technique*. in *the 18th International Symposium on Power Semiconductor Devices & IC's*. 2006. Naples, Italy.
6. Zhang, Z., and G-Q. Lu, *Pressure-Assisted Low-Temperature Sintering of Silver Paste as an Alternative Die-Attach Solution to Solder Reflow.* IEEE Transactions on Electronics Packaging Manufacturing, 2002. **25**(4): p. 279 - 283.
7. Scheuermann, U., and P. Beckedahl, *The Road to the Next Generation Power Module - 100% Solder free Design*, in *The 5th International Conference on Integrated Power Electronics Systems (CIPS 2008)*. 2008: Nuremberg, Germany.
8. Scheuermann, U., *Reliability challenges of automotive power electronics.* Microelectronics Reliability, 2009. **49**: p. 1319-1325.
9. Bai, J.G., and G-Q. Lu, *Thermomechanical Reliability of Low-Temperature Sintered Silver Die-Attached SiC Power Device Assembly.* IEEE Trans. on Device and Materials Reliability, 2006. **6**(3): p. 436 - 441.
10. Bai, J.G., Z. Z. Zhang, J. N. Calata, and G-Q.

Lu, *Low-Temperature Sintered Nanoscale Silver as a Novel Semiconductor Device-Metallized Substrate Interconnect Material.* IEEE Transactions on Components and Packaging Technologies 2006. **29**(3): p. 589 - 593.

11. Zhang, Z., J. N. Calata, J. G. Bai, and G-Q. Lu. *Nanoscale Silver Sintering for High-Temperature Packaging of Semiconductor Devices*. in *Proc. of 2004 TMS Annual Meeting & Exhibition*. 2004. Charlotte, NC.
12. Bai, J.G., J. N. Calata, G. Lei, Z. Zhang and G-Q. Lu. *Thermomechanical Reliability of Sintered Silver Die-attachment*. in *the 10th Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITHERM)*. 2006. San Diego, CA.
13. G. B. Stringfellow and M. G. Craford, " High Brightness Light Emitting Diodes: Volume 48", Academic Press, 1997.
14. S. Naritsuka, Y. Nishikawa, H. Sugawara, M. Ishikawa and Y. Kokubun, " Studies on InGaAlP Layers Grown by Low-Pressure Metalorganic Chemical Vapor Deposition Photoluminescence", Journal of Electronic Materials, 1991, Vol. 20, No. 9.
15. J.G. Liu et al, "Chip-on-Board Packaging and Thermal Solutions for 100W Single Large Area LED" IMAPS 5th International Conference and Exhibition on Device Packaging, Scottsdale AZ, March 9-12, 2009.
16. A.A. Erchak et al., "Patterned Light Emitting Devices," US Patent, US7,345,416 B2. Mar. 18, 2008
17. R. Karlicek, "Photonic Lattice LEDs are New Class of Light-Emitting Device," LEDs Magazine, July/August, pp 20-23, 2007.
18. A.A. Erchak et al., "Enhanced Coupling to Vertical Radiation Using a Two-Dimensional Photonic Crystal in a Semiconductor Light-Emitting Diodes," Appl. Phys. Lett. 78(5), pp. 563-565, 2001.
19. A.A. Erchak, "PhlatLight: the Future of Rear Projection TVs," 4th Annual DisplaySearch HDTV Conf., Aug 2006.
20. C. Hoepfner, "PhlatLight™ Photonic Lattice LEDs for RPTV Light Engines," SID Symposium Technical Papers, Vol. 37, pp. 1808-1811, 2006.
21. J. E. Sergent and A. Krum, "Thermal Management Handbook for Electronic Assemblies," McGraw-Hill, New York, 1998.
22. M. Denninger, "A General Solution Framework for LED Cooling Problems," IMAPS New England 35th Symposium and Expo, Boxborough, MA, 2008.
23. R. Karlicek, J. Graff, and D. Sciabica, "Thermal Design Considerations for High-Power Single-Chip LEDs," LEDs Magazine, January/February pp 40-43, 2008.