"Development of a Double-side Cooled Power Module Joined by Low-temperature Sintering of Nanosilver Paste for Electric Vehicles"

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Abstract

In present electric vehicles (PHEV/HEV/EV), an extra cooling loop is needed to lower the power-electronics coolant temperature below about 65°C from the radiator coolant temperature of 105°C. One way to reduce the cost of future EVs is to eliminate the extra cooling loop by developing reliable high-temperature power inverter modules that are sufficiently cooled by the radiator coolant. This calls for the development of power packaging technologies that can enable silicon and/or SiC power devices working at junction temperature in excess of 175°C. In the current phase of our power packaging research effort, we have focused on replacing the solder-reflow technique for die-attaching power chips by an emerging low-temperature joining technology (LTJT) which involves low-temperature sintering of silver powders. To reduce the process complexity of the conventional LTJT arising from the need of high pressure (30 to 40 MPa or 300 to 400 Kg-force per cm^2), we used a nanosilver paste material to lower the die-attach temperature below 270°C with zero or less than 5 MPa pressure. This simplified LTJT is less likely to damage the chips and allows us to implement a planar packaging scheme for interconnecting both sides of the power devices without using wire bonds. The planar power modules have low parasitic inductances thus less ringing noises from the device-switching action and can be cooled from both sides of the devices for improved thermal management. Details on design and packaging of a double-side cooled power modules and preliminary test results on its electrical performance are presented.

Keywords: Electric vehicles; Double-side cooled power module; Low-temperature sintering; Nanosilver paste

I. Introduction

Hybrid electric vehicles and plug-in hybrid-electric vehicles represent a promising solution to cut down global carbon emission and lower petroleum consumption. Thus, all the major automotive makers are actively working on plans to increase the percentage of electric vehicles in their future production. The US Department of Energy (DOE) has been partnering with US automakers to develop technologies that would make HEVs and PHEVs cost effective to consumers. According to a cost-benefit study [1] funded by DOE, the reduction in petroleum use can exceed 45% per PHEV equipped with 20 mi (32 km) or more of energy storage. However, the long-term incremental costs of these vehicles are projected to exceed $8,000, with near-term costs being significantly higher. One solution to reduce the costs of HEVs and PHEVs is to eliminate an extra cooling loop required for lowering the 105°C-coolant exiting the radiator to 65°C, which is necessary to cool today's power electronics inverter modules. Realization of this solution demands the development of power electronics that can function reliably at chip junction temperature over 175°C.

Today, chips in power modules are joined to substrate using a lead-free or high-lead solder paste or solder preform films by following the solder-reflow process at temperatures from 260°C to over 300°C to melt and then solidify the solder alloy. After the chips are soldered, their top terminals are connected by ultrasonic bonding of aluminum wires or ribbons. This scheme of chip interconnection limits the heat dissipation to one side, namely through the poorly conducting solder layer, and presents serious concern on solder-joint reliability. Solder alloys generally have low electrical and thermal conductivity, and the soldered chip joints are known to fail by fatigue under cyclic loading because of low yield strength and accumulation of high inelastic strains during deformation. This concern for the joint reliability becomes more critical if the junction temperature is to go over 175°C.

Consequently, in the quest for high-temperature

power packaging technologies, the foremost challenge to overcome is to replace the solder interconnection with a die-attach technology that: (1) can be processed at low temperature (below 300°C) in short time for low cost; (2) has high thermal and electrical conductivity for performance; (3) has a low homologous temperature ($T/T_{melting}$) and low elastic modulus for joint reliability; and (4) is easy to implement double-sided cooling to reduce the junction temperature swing (ΔT) for further improving reliability.

A low-temperature joining technology (LTJT) based on sintering of silver powders has emerged in the power electronics industry. Semikron, a leading manufacturer of power modules in Europe, has a manufacturing line using LTJT. They claimed to achieve, with the sintered chip-attachment, 5x higher temperature cycling capability, 3x better total module resistance, and device junction temperature up to 175°C. Other major companies in Europe, such as Danfoss, Infineon, and Volkswagen are also evaluating the low-temperature sintering technology for assembling their power modules. However, a roadblock for implementing the technology is the requirement of pressure, 30 to 40 MPa or 300 to 400 kg-force on a 100 mm^2 chip, to lower the silver sintering temperature from over 700°C down to about 250°C [2-4]. This limits production throughput, complicates manufacturing process, and places critical demands on substrate flatness and thickness of the chips.

The recent development of a nanosilver paste [5-9] that can be sintered with zero or pressure less than 5 MPa is promising for speeding up the LTJT implementation. In this paper, we report the use of this enabling nanomaterial for making planar, double-side cooled power modules and some preliminary electrical results of the module tested at high junction temperature.

II. Module layout and assembly

Fig. 1 is a schematic of a planar, double-side cooled half-bridge power module assembled in this study. Power module layout has a significant impact on parasitic inductances, which are responsible for voltage spikes in switching operations. To minimize the commute loop and drive loop ESLs, a symmetrical design of the layout with minimal circular loop area was selected. The on-module capacitors and current sensor are used for testing purpose. Fig. 2 is a picture of all the components, except the dc-link capacitors and current sensors, for making the planar power module. Copper plates of 0.25-mm thick were used to join the source terminal of the IGBT and anode side of the diode, as opposed to the conventional wire-bonding approach, accomplishes the planar interconnection and facilitates heat transfer from both sides of the devices. The IGBT and diode chips were purchased from IXYS Corporation, and they were metalized with silver on all the terminals. They are older generation devices rated at 1200 V and 70 A for the IGBT and 1200 V and 100 A for the diode. Because the IGBT and diode have different thickness, copper shims were used to ensure leveled planar interconnection of the copper plate on top of the chips. They also help increase the breakdown voltage by raising the gap between the devices and Cu plates. The copper bars were used to connect the copper plates to the direct-bond-copper substrate.

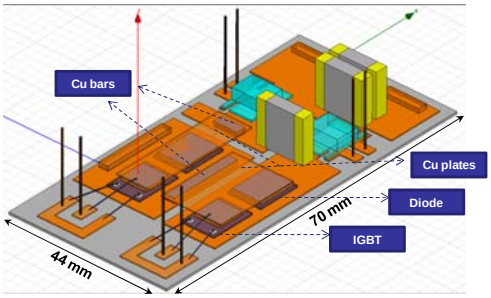


Fig. 1. Schematic design of a planar, double-side cooled power electronic module.

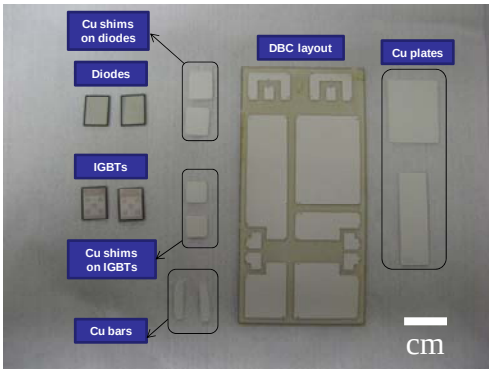
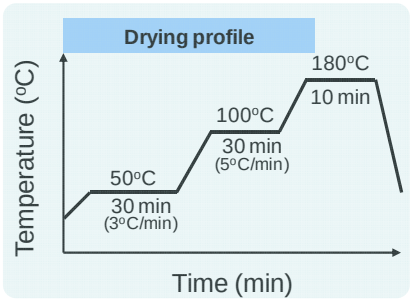


Fig. 2. Display of various components, excluding the DC-link capacitors and current sensor chips, for making the power module.

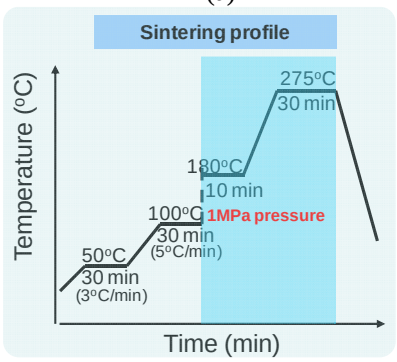
The surfaces of all the components in Fig. 2 were coated with silver, either by vapor-phase deposition or electroplating, making them compatible with the joining technology via silver sintering. The silver paste used to assemble the planar power module was acquired from NBE Technologies, LLC (www.nbetech.com). It consists of nanoparticles of silver in an organic formulation.

To build the power module, we applied the nanosilver paste on all the joints by stencil-printing and then followed the drying and sintering profiles

depicted in Fig. 3. Since some of the joint areas are larger than 5 x 5 mm, we used a double-print process consisting of: (1) applying layers of the paste on joints; (2) drying them to remove most of the organics by the drying profile; (3) applying another thin layers of the paste on the dried layers; (4) attaching the pieces; (5) heating the assembled part by the sintering profile; and (6) adding 1 MPa pressure when temperature reached 180°C. Fig. 4 is a photo of a fully assembled planar module.



(a)



(b)

Fig. 3. Time-temperature heating profiles used for (a) drying the initial layers of the paste and (b) sintering the joints together.

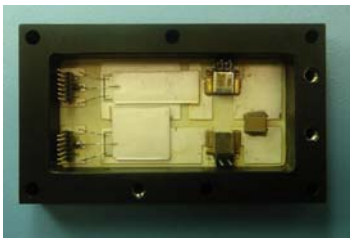


Fig. 4. A fully assembled power module with planar interconnection on top of the devices to achieve double-sided cooling thermal management.

III. Electrical testing of the module

A preliminary electrical evaluation of the assembled power module was done by a double-pulse test shown in Fig. 5. The double-pulse test usually is used to measure the switching characteristics of power modules. Table I lists the sequence of the testing procedure. Since the devices in the module are older generations and the switching behavior is not the main concern here, we used the double-pulse test to demonstrate the switching operation at high device junction temperature.

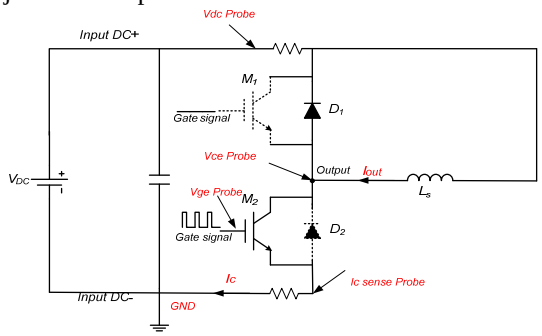


Fig. 5. A schematic diagram of the double-pulse test.

Table I: Double-pulse testing procedure.

Phase I	IGBT is on; L_s is linearly charged by V_{DC}. L_s current increases linearly.
Transient I	IGBT is being turned off, and diode is being forced to turn on. L_s current is being diverted into diode from IGBT. The turn-off characteristics of the IGBT module, i.e. turn-off time, voltage spike, turn-off energy, at initial conditions of Ic and Vdc, could be measured during this transient period.
Phase II	IGBT is off; L_s current is freewheeling through the diode and is held to be constant.
Transient II	IGBT is turning on; diode is being forced to shut down. L_s current is being diverted into IGBT from diode. The turn-on characteristics of the IGBT module, i.e. turn-on time, voltage spike, turn-on energy, at initial conditions Ic and Vdc, could be measured during this transient period.
Phase III	IGBT is on; L_s is linearly charged by V_{DC}.

In a typical double-pulse test, the devices are not heated since the switching pulses are short. To get high junction temperature, we placed the module on a hot plate to raise the case temperature and added a heating pulse to the devices prior to the double-pulse test. To avoid melting the solder joints on a testing board that had to be closely connected to the module, we limited the module case temperature to 150°C, and then controlled the heating pulse to raise the chip temperature by about 25°C. So, during the switching

test, the chip junction temperature was at around 175 ºC. Fig. 6 shows the switching waveforms of the module at the high junction temperature. Efforts are underway to characterize the thermal performance and reliability of the module.

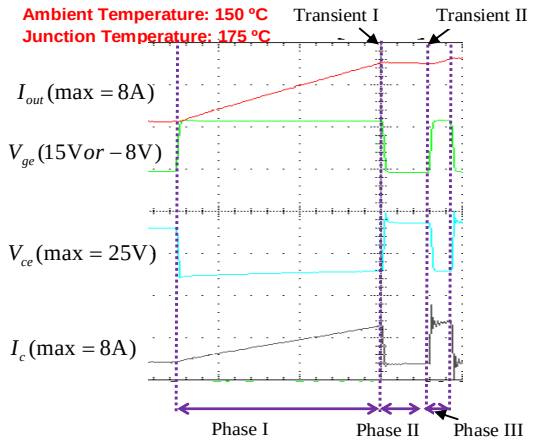


Fig. 6. Switching waveforms of the module tested at 150°C case temperature and 175°C junction temperature.

IV. Summary

A planar device-interconnection design was presented for making power modules that are capable of double-sided cooling. In addition, by using the low-temperature joining technology with a nanosilver paste, we demonstrated that the modules could be made by a low-pressure process to support switching operations at high junction temperatures.

Acknowledgment

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V. References

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